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KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

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PIZARRO CRESPO, MARCOS D	

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/646,103
Filing Date: August 22, 2003
Appellant(s): LIU ET AL.

Michael S. Okamoto, reg. No. 47,831
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed on 10/17/2005 appealing from the Office action mailed 4/19/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,496,759	YUE	3-1996
5,861,328	TEHRANI	1-1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 2, 4, 8, 9, 12-14, 16, 17, 19, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Tehrani (US 5861328).

Regarding claim 1, Tehrani shows (see, *e.g.*, figs. 4-8) all aspects of the instant invention including a process for passivating a magneto-resistive bit **41** having a top surface and side walls characterized by encapsulating the top and side wall surfaces of the bit **41** with a conductive etch stop barrier layer.

Regarding claim 2, Tehrani shows the conductive barrier layer comprising CrSi (see, *e.g.*, col.6/ll.1).

Regarding claim 4, Tehrani shows the method further comprising forming a diffusion barrier between the conductive barrier layer and the top surface and sidewalls of the bit (see, *e.g.*, col.6/ll.2).

Regarding claim 8, Tehrani shows (see, *e.g.*, figs. 4-8) all aspects of the instant invention including a process for passivating a magneto-resistive bit structure characterized by the steps of:

- ✓ Providing a GMR stack **35** upon a substrate
- ✓ Selectively patterning the GMR stack **35** to form one GMR bit **41** having a top surface and side walls
- ✓ Providing an conducive etch-stop barrier layer that encapsulates the patterned GMR stack **35** including the top surface and sidewalls of the bit (see, *e.g.*, fig. 5)

- ✓ Selectively patterning the etch-stop layer so that edges of the layer extend out past the edges of the GMR bit **41** (see, *e.g.*, fig. 6)

Regarding claim 9, Tehrani shows the process further comprising forming a diffusion barrier between the etch-stop layer and the patterned GMR stack (see, *e.g.*, col.6/ll.2).

Regarding claim 12, Tehrani (see, *e.g.*, figs. 4-8) shows a process for passivating a patterned magneto-resistive bit structure in a magneto-resistive memory, the process comprising:

- ✓ Providing a substrate with the patterned magneto-resistive bit structure **41**, the bit **41** having a top surface and side walls
- ✓ Forming a conductive etch-stop barrier layer over the substrate, the etch-stop layer covering the top surface and side walls of the bit (see, *e.g.*, fig. 5)
- ✓ Patterning the etch-stop layer such that it is removed from portions of the substrate but it remains on the top surface and around the side walls of the bit structure (see, *e.g.*, fig. 6)

Regarding claim 13, Tehrani shows the substrate further comprising a monolithic integrated circuit (see, *e.g.*, col.2/ll.28-40).

Regarding claim 14, Tehrani shows the etch-stop layer comprising CrSi (see, *e.g.*, col.6/ll.1).

Regarding claim 16, Tehrani shows the process further comprising forming a diffusion barrier before forming the etch-stop layer such that the diffusion barrier is formed between the etch-stop layer and the substrate (see, *e.g.*, col.6/ll.2). Tehrani

further shows that patterning the etch-stop layer further comprises patterning the diffusion barrier (see, *e.g.*, fig. 6).

Regarding claim 17, Tehrani shows the diffusion barrier comprises Ta (see, *e.g.*, col.6/ll.2).

Regarding claim 19, Tehrani shows the diffusion barrier comprises TaN (see, *e.g.*, col.6/ll.2).

Regarding claim 20, Tehrani shows the process further comprising forming a diffusion barrier comprising Ta before the etch-stop layer such that the diffusion barrier is formed between the etch-stop layer and the substrate (see, *e.g.*, col.6/ll.2). Tehrani further shows the etch stop layer comprising CrSi (see, *e.g.*, col.6/ll.1), the substrate comprising a monolithic integrated circuit (see, *e.g.*, col.2/ll.28-40), and that patterning the etch-stop layer comprises patterning the diffusion barrier (see, *e.g.*, fig. 6).

Claims 3, 5-7, 10, 11, 15, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tehrani in view of Yue (US 5496759).

Regarding claims 3 and 15, Tehrani shows most aspects of the instant invention (see, *e.g.*, paragraphs above). He, however, fails to specify the thickness of the etch-stop layer. However, differences in thickness will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such thickness and/or concentration are critical. "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the workable ranges by routine experimentation". *In re Aller*, 220 F.2d 454,456,105 USPQ 233, 235 (CCPA 1955).

Since the applicants have not established the criticality (see next paragraph) of the etch-stop thickness, and since the claimed thickness of 300 Å is in common use in similar devices in the art (see, *e.g.*, Yue/col.2/ll.42), it would have been obvious to one of ordinary skill in the art to use these values in the device of Tehrani.

CRITICALITY

The specification contains no disclosure of either the critical nature of the claimed thickness or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Regarding claim 5, Tehrani shows the diffusion barrier comprises Ta (see, *e.g.*, col.6/ll.2).

Regarding claims 6 and 18, Yue shows the diffusion barrier is about 100 Å (see, *e.g.*, col.2/ll.40). See also the comments stated about with respect to claims 3 and 15, which are considered repeated here.

Regarding claim 7, Tehrani shows the diffusion barrier comprises TaN (see, *e.g.*, col.6/ll.2).

Regarding claim 10, Tehrani shows most aspects of the instant invention (see, *e.g.*, paragraphs above). He also shows that the step of selectively patterning the etch-stop layer includes forming a dielectric layer upon the etch-stop layer and removing portions of the dielectric layer and the etch-stop layer (see, *e.g.*, figs. 5 and 6). He, however, fails to specify that the step of removing parts of the dielectric layer exposes portions of the etch-stop layer to be removed, and that the step of removing the etch-stop layer includes ion milling to remove the exposed portions of the etch-stop layer.

Yue (see, *e.g.*, col.3/ll.53-58), on the other hand, teaches that doing so would result in Tehrani having very well defined via openings with a very smooth opening edge.

It would have been obvious at the time of the invention to one of ordinary skill in the art to have the step of removing parts of Tehrani's dielectric layer to expose portions of the etch-stop layer and to subsequently ion mill the exposed portions of the layer, as suggested by Yue, because doing so would result in very well-defined via openings with very smooth edges.

Regarding claim 11, Tehrani (see, *e.g.*, col.5/ll.32) teaches that the dielectric layer may be removed using reactive ion etching.

(10) Response to Arguments

The appellants argue:

Tehrani teaches two distinct processes, a process with a dielectric barrier and a process suitable for a conductive etch stop barrier layer, but only illustrates the process with the dielectric barrier in the figures. The examiner is improperly mixing the teachings of the process suitable for the conductive barrier (not illustrated) with the teachings of the process with the dielectric barrier (illustrated). The claimed invention requires sidewalls of a magnetoresistive bit to be encapsulated by a conductive etch stop barrier layer. The examiner applied a conductive barrier teaching of Tehrani and improperly combines it with another Tehrani process in which sidewalls of a bit are exposed prior to forming a dielectric barrier. In fact the two processes are separate and incompatible. The first process with the dielectric barrier is illustrated in figures 5, 6, and 7 and described in col.4/ll.66-col.5/ll.53. In said first process via openings 47 and 50 are formed in separate operations. The second process with the conductive barrier is described in col.5/ll.54-col.6/ll.12 and it is not shown. In said second process the vias 47 and 50 are formed in a single operation. Tehrani explicitly teaches that two distinct processes are taught by the use of the term "either" in col.6/ll.13-14, which indicates two exclusive alternatives.

The examiner responds:

Tehrani is using his figures to describe both processes. Otherwise, why would Tehrani use the same reference numbers to refer to the same features in his description of both processes. The examiner agrees with the appellants that Tehrani uses figures 5-8 to describe the first process. Tehrani, however, does not provide any other figures, besides figures 5-8, in his description of the second process, yet he uses the same

reference numbers (see, *e.g.*, col.5/ll.54-col.6/ll.12). That the figures referred to both processes is evinced in the fact that Tehrani uses the same reference numbers in his description of both processes and that he clearly indicates so when referring to figure 8 as applying to both processes (see, *e.g.*, col.6/ll.13-17).

In any event, Tehrani clearly sets forth what are the differences between both processes. That is, in the first process vias 47 and 50 are formed in separate steps, as illustrated in figures 6 and 7 (see, *e.g.*, col.5/ll.22-35), whereas in the second process vias 47 and 50 are formed in a single operation (see, *e.g.*, col.5/ll.54-55). In that regard, figures 6 and 7 will be particular to the first process but only for its showing of forming vias 47 and 50 in two separate method steps. In any event, "[A]fter the formation of vias 47 and 50, by either of the above described means" (see, *e.g.*, col.6/ll.13-14), both processes will continue, "[a]s illustrated in FIG. 8" (see, *e.g.*, col.6/ll.16-17).

The appellants argue:

> Tehrani admonishes against a combination of the two processes. With respect to the first process via openings 50 may overlap GMR element 41, that is, vias 50 may extend outside or intersect the end of the GMR element 41 (see, *e.g.*, col.5/ll.36-38). In contrast, with respect to the second process, Tehrani states that via openings 50 must be enclosed by GMR element 41, that is, the contact may not extend outside the ends of the GMR memory 41 to protect element 41 from the resist stripping processes and other oxidizing or corrosive agents (see, *e.g.*, col.5/ll.58-62).

The examiner responds:

Tehrani clearly sets forth the differences between both processes. Setting forth the differences between both processes is not the same as admonishing against combining both processes. The two processes are very similar to each other with one step difference. In the first process, vias 47 and 50 are formed in separate steps (see, *e.g.*, col.5/ll.34-35). In the second process vias 47 and 50 are formed in a single operation (see, *e.g.*, col.5/ll.54-55). In the first process, because of the requirements to

protect the bit, the vias 47 are formed first (see, *e.g.*, col.5/ll.25-27). Subsequent to forming the vias 47, the vias 50 are formed (see, *e.g.*, col.5/ll.35). Because of the two separate process steps used to form vias 47 and 50, vias 50 may extend outside the bit 41 (see, *e.g.*, figs. 6-7 and col.5/ll.25-38). On the other hand, in the second process, Tehrani combines forming vias 47 and 50 in one single operation. Now that vias 47 are formed together with vias 50, Tehrani restrict forming the vias 50 so that the contacts may not extend outside the ends of the bit to better protect the bit 41 (see, *e.g.*, col.5/ll.54-62).

That both processes are very similar to each other is evinced in the fact that Tehrani clearly indicates that "[A]fter the formation of vias 47 and 50, by either of the above described means" (see, *e.g.*, col.6/ll.13-14), both processes will continue, "[a]s illustrated in FIG. 8" (see, *e.g.*, col.6/ll.16-17).

The appellants argue:

> Tehrani teaches two distinct processes, the first process uses a dielectric barrier and the second process uses a conductive barrier. In the first process Tehrani uses silicon nitride as a barrier layer, a second SiO2 layer, and an optional third layer of AlO or AlN as an etch stop layer for the dielectric cap 45 (see, *e.g.*, col.5/ll.3-21). None of these materials are conductive. In the second process he uses CrSi as a conductive barrier layer.

The examiner responds:

Tehrani teaches that the cap layer 45 is a dielectric layered system and he specifically refers to it as the dielectric cap layer 45 in his description of both processes (see, *e.g.*, col.5/ll.4 and col5/ll.57-58). This dielectric cap 45 completely seals the bit structure 41 and provides a barrier to moisture, oxidation, and corrosive agents (see, *e.g.*, col.5/ll.1-4 and figure 5). This is also illustrated in figure 5, where Tehrani shows the cap layer 45 sealing the bit structure 41. The difference between the cap layer of

the first and second processes is that the first layer of the dielectric cap 45 in the second process is a conductive etch stop barrier layer (see, *e.g.*, col.5/ll.55-58 and col.5/ll.67-col.6/ll.2).

The appellants argue:

> In the second process, Tehrani states that vias 50 must be enclosed by GMR element 41, *i.e.*, that the contact may not extend outside the ends of bit 41. As he further describes, where the etch stop and passivation layer is conductive, contact metal can be simply deposited in contact therewith in vias 50 (see, *e.g.*, col.6/ll.9-12). Thus, when Tehrani describes a conductive etch stop barrier layer, the layer explicitly does not encapsulate the sidewalls.

The examiner responds:

The two processes are very similar to each other with one step difference. In the first process, vias 47 and 50 are formed in separate steps (see, *e.g.*, col.5/ll.34-35). In the second process vias 47 and 50 are formed in a single operation (see, *e.g.*, col.5/ll.54-55). In the first process, because of the requirements to protect the bit, the vias 47 are formed first (see, *e.g.*, col.5/ll.25-27). Subsequent to forming vias 47, vias 50 are formed (see, *e.g.*, col.5/ll.35). Because of the two separate process steps used to form vias 47 and 50, vias 50 may extend outside the bit 41 (see, *e.g.*, col.5/ll.25-38). That is because the bit 41 is protected while vias 47 are formed (see, *e.g.*, col.5/ll.27-33). On the other hand, in the second process, Tehrani combines forming vias 47 and 50 in one single operation. Now Tehrani will use the same etchants, chemicals, and corrosive materials that he used to form vias 47 (see, *e.g.*, col.5/ll.27-33) to form vias 50. To better protect the bit 41, Tehrani restrict forming the vias 50 so that the contacts may not extend outside the ends of the bit (see, *e.g.*, col.5/ll.58-62).

Regarding both processes, Tehrani teaches that the cap layer 45 is a dielectric layered system and he specifically refers to it as the dielectric cap layer 45 in his

description of both processes (see, *e.g.*, col.5/ll.4 and col5/ll.57-58). This dielectric cap 45 completely seals the bit structure 41 and provides a barrier to moisture, oxidation, and corrosive agents (see, *e.g.*, col.5/ll.1-4 and figure 5). As he further explains, it is the first layer of the dielectric system that completely seals the bit structure 41 (see, *e.g.*, col.5/ll.4-8). This is also illustrated in figure 5, where Tehrani shows the cap layer 45 sealing the bit structure 41. Tehrani also sets forth the differences between the cap layer of the first and second processes, *i.e.*, that in the first process the first layer of the dielectric cap is an insulating barrier and that in the second process the first layer of the dielectric cap 45 is a conductive etch stop barrier layer (see, *e.g.*, col.5/ll.4-9, col.5/ll.55-58 and col.5/ll.67-col.6/ll.2).

Appellants conclusion that the etch stop barrier layer does not encapsulate the sidewalls of the bit because the vias 50 may not extend outside the bit is not described by Tehrani. What it is clearly described in Tehrani is the fact that first layer of the cap layer 45 completely seals the bit 41 (see, *e.g.*, col.5/ll.4-8) and that in the second process, this first layer is CrSi, which is a conductive material (see, *e.g.*, col.5/ll.55-58 and col.5/ll.67-col.6/ll.2).

The appellants argue:

> The examiner relies on Tehrani's figure 6 as support for the assertion that Tehrani teaches selectively patterning the etch-stop layer so that edges of the layer extend out past the edges of the GMR bit 41 (see, e.g., fig. 6). Figure 6 applies only to Tehrani's dielectric barrier process and not to Tehrani's conductive barrier process. The appellants note that figure 6 illustrates only vias 47. Vias 50 are not present until next figure 7. In the first process, vias 47 and 50 are formed in separate steps (see, *e.g.*, col.5/ll.34-36), whereas in the second process, the vias are formed in a single operation (see, *e.g.*, col.5/ll.54-55). Accordingly, in the conductive barrier layer process, figure 6 does not apply.

The examiner responds:

The examiner agrees with the appellants that figures 6 is depicting a step that is particular to the first process, *i.e.*, that the vias 47 and 50 are formed in different steps. The examiner, however, used figure 6 to better illustrate the patterning step of the etch stop layer, which is the first layer of dielectric cap 45 of the second process (see, *e.g.*, col.5/ll.57-58). As previously indicated, the two processes are very similar to each other with one step difference. In the first process, vias 47 and 50 are formed in separate steps (see, *e.g.*, col.5/ll.34-35). In the second process vias 47 and 50 are formed in a single operation (see, *e.g.*, col.5/ll.54-55). Common to both processes, however, is the fact that the vias 47 are formed. That is, both processes show the patterning of the cap layer 45 to form vias 47. This is evinced in figure 8, which clearly refers to both processes (see, *e.g.*, col.6/ll.13-18), showing vias 47. Since in the second process the first layer of dielectric cap 45 is the conductive etch stop layer, patterning vias 47 will then means patterning all the layers making up the dielectric cap 45 including also the first layer, which is the conductive etch stop layer. Therefore, the patterning step of the vias 47 as illustrated in figure 6, which will also takes place in the second process, more clearly illustrates the claim limitation of patterning the etch stop layer so that the edges of the layer extend out past the edges of the bit 41. In other words, the examiner is not relying on figure 6 for its illustration of patterning vias 47 and 50 in separate steps, but for its clear illustration of patterning the vias 47 as they are also patterned in the second process.

The appellants argue:

The examiner acknowledges that Tehrani does not specify the thicknesses of the etch-stop layer and the tantalum diffusion barrier. The examiner then uses Yue to provide the missing thicknesses and raised the issue of criticality. Neither Tehrani nor Yue recognizes the criticality of the thicknesses of either material. The thickness of

the CrSi layer and/or Ta layer is important, as it relates to the resistivity of the material that is shunting the bit. If the materials are too thick, the bit is effectively shorted by the CrSi layer.

The examiner responds:

The examiner's appreciate appellant's effort to establish the criticality of the claimed thicknesses. However, appellants' statements that the claimed thickness is important as it relates to the resistivity of the material fail to overcome the rejection of the claims. To be of probative value, appellants' assertion should be supported by actual proof. The MPEP gives guidelines on how to demonstrate the criticality of a claimed range. See, *e.g.*, MPEP§716.02(d). As explained therein, the appellants should compare a sufficient number of tests both inside and outside the claimed range to show the criticality of the range. The evidence relied upon should establish "that the differences in results are in fact unexpected and unobvious and of both statistical and practical significance." *Ex parte Gelles*, 22 USPQ2d 1318, 1319 (Bd. Pat. App. & Inter. 1992). The appellants, however, have failed to present any data showing that having a CrSi layer of about 300 angstroms and having a Ta layer of about 100 angstroms is critical. Due to the absence of said data, the examiner concludes that appellants' assertion that the claimed thicknesses are critical constitutes mere argument. Therefore, since the appellants have failed to establish the criticality of the claimed thicknesses of the barrier layers, and since similar thicknesses have been used in similar processes in the art (see, *e.g.*, Yue/col.2/ll.40-42), and since the cited art shows all other limitations in the claims, it would have been obvious to one of ordinary skill in the art to use the claimed values in the device of Tehrani.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

An appeal conference was held on 12/13/2005 between Mr. Marcos D. Pizarro (Patent Examiner), Mr. Darren Schuberg (Supervisory Patent Examiner), and Mr. Wael Fahmy (Supervisory Patent Examiner) as the conferees.

Respectfully submitted,

Darren Schuberg
Supervisory Patent Examiner
Art Unit 2834

Wael Fahmy
Supervisory Patent Examiner
Art Unit 2814

Marcos D. Pizarro
Patent Examiner
Art Unit 2814
(Tel) 571-272-1716